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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/621,110	07/21/00	COHN C	6-4

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DOCKET ADMINISTRATOR ROMM 3C-512
LUCENT TECHNOLOGIES INC
600 MOUNTAIN AVENUE
P O BOX 636
MURRAY HILL NJ 07974-0636

EXAMINER
LUU,C

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/09/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/621,110	COHN ET AL.	
	Examiner	Art Unit	
	Chuong A Luu	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 1-9, and 12-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Ma (U.S. 6,022,787)

Ma discloses a method of making an integrated circuit by

(1); (7); (8); (17) (a) providing a substrate 122 having a first dielectric layer 124, a conductive layer 126 above the first dielectric layer 124 (see Figure 8), and a second

dielectric layer 128 above the conductive layer 126 (see Figure 9), the second dielectric layer 128 having a cavity 134, 136 exposing a portion of the conductive layer 126 (see Figure 12); (b) interconnecting 150, 152 an integrated circuit directly to the exposed portion of the conductive layer 126 in the cavity 134, 136 (see Figures 13, 14); **(6)** further comprising forming multiple interconnections between the integrated circuit chip and the conductive layer (see columns 7, 8, lines 33-67, and lines 1-44, respectively);

(2) wherein step (b) comprises: coupling a conductor 154 to a bond pad formed on the integrated circuit; connecting the conductor 154 directly to the conductive layer; **(12); (13)** coupling the integrated circuit chip to the substrate (see column 8, lines 45-51. Figure 15);

(3) further comprising providing one of a ground plane and a power plane in the exposed portion of the conductive layer; **(4)** further comprising providing at least one connection for a signal line in the exposed portion of the conductive layer; **(5)** further comprising providing at least one connection for a signal line in the exposed portion of the conductive layer; **(9)** further comprising: providing a contact area to a ground plane by exposing the portion of the conductive layer (see columns 4, 9, lines 33-43, lines 15-30, respectively);

(13) (a) providing a first dielectric layer 124; (b) providing a first conductive layer 126 above the dielectric layer 124 (see Figure 8); (c) providing a second dielectric layer 128 above the first conductive layer 126 (see Figure 9); (d) providing a second conductive layer 130 above the second dielectric layer 128 (see Figure 10); (e) forming a cavity 134, 136 in a first region of the second dielectric layer 128 to expose a portion

of the first conductive layer 126 (see Figure 12); **(14)** wherein step (d) further comprises providing the second conductive layer 130 on regions other than the first region; **(15)** wherein step (d) further comprises removing a portion of the conductive layer formed above the first region (see columns 7, and 8, lines 33-67, and lines 1-44, respectively).

Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma (U.S. 6,022,787) in view of Caillat et al. (U.S. 5,861,322)

Ma teaches the above outlined features except for forming plated through holes in the substrate. However, Caillat discloses a process for manufacturing an interconnection substrate (see column 2, lines 1-36). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the above teachings to manufacture a semiconductor interconnection to improve its performance.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ma, and Caillat et al. disclose a method of making an integrated circuit. However, the following references Wong (U.S. 6,027,999); Lee (U.S. 6,277,705 B1); Yamaji et al. (U.S. 6,159,837); Rolfson (U.S. 6,200,889 B1); Rolfson (U.S. 6,060,378) can be applied in the next office action..

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A Luu whose telephone number is (703)305-0129. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703)308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Chuong Anh Luu
Assistant Examiner

CAL
October 19, 2001

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800